IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A testing apparatus having probes to be brought into contact with electrodes of a semiconductor device as a test, comprising:

a plurality of double-support beams supported by support portions of a substrate, wherein said probes are formed on said beams; and

first lines to connect said probes to secondary electrodes formed on said substrate and second lines to connect said beams to said support portions, wherein said first and second lines are formed on said beams.

2. (Original) A testing apparatus having probes to be brought into contact with electrodes of said semiconductor device as a test, comprising:

a plurality of double-support beams that are supported by support portions of a substrate, wherein said probes are formed on said beams; and

lines to connect said probes to secondary electrodes formed on said substrate;

wherein each said line is formed on one of said double-support beams and extends from both sides of one of said probes on a face of said beam where said probe is formed.

3. – 5. (Cancelled)

6. (Original) A testing apparatus for testing a semiconductor device, comprising:

a plurality of double-support beams supported by support portions of a silicon substrate;

probes that are projections formed on said beams and to be brought into contact with electrodes of said semiconductor device as a test subject; and

wiring lines that connect said probes to secondary electrodes formed on said silicon substrate, wherein said wiring lines are formed on a face of said double-support beam where said probes are formed, so as to extend to two support portions at both ends of said beam.

7. (Cancelled)

8. (Original) The testing apparatus according to claim 1;

wherein each said probe formed on one of said beams is distanced from and adjacent probe formed on an adjacent beam by 100 μm or less.

9. – 10. (Cancelled)

11. (Original) A semiconductor device manufacturing method comprising;

a test process including at least one of a characteristics test process;

an initial defect accelerated selection test process; and

a final performance test process that are to be executed on LSIs formed on a wafer or individual LSIs obtained by cutting a wafer;

wherein said test process is executed by using a testing apparatus comprising:

a plurality of double-support beams supported by support portions of a silicon substrate,

probes formed on said beams and to be brought into contact with electrodes of an LSI as a test subject,

wiring lines to connect the probes to secondary electrodes formed on said silicon substrate, wherein said wiring lines are formed on a face of said double-support beams where said probes are formed and extend to said two support portions at both ends of said beam.

12. – 13. (Cancelled)

14. (Original) A testing apparatus according to claim 1, wherein said beams are double-support beams, said first lines are located on a first side of said probes, and said second lines are located on another side of said probes on a front face of said double-support beams.

15. - 16. (Cancelled)

17. (New) A testing apparatus according to claim 1, wherein said first lines are formed on said substrate and extended through through-holes formed in said support portions to connect said probes to said secondary electrodes, and said first and second lines are formed on faces of said beams when said probes are formed.

18. (New) A testing apparatus according to claim 17, wherein said secondary electrodes are formed on said substrate to face in a direction opposite to said faces of said beams where said probes are formed.